


FORM PTO-1449 MODIFIED		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		Application Number	09/705,395
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date	November 2, 2000
				First Named Inventor	Jonathan S. Turner
				Group Art Unit	2662
				Examiner Name	PATEL, AJIT
Sheet	1	of	1	Attorney Docket No.	52186

U.S. PATENT DOCUMENTS				
EXAMINER'S INITIALS	Cite No.	Document Number	ISSUE or PUBL. DATE	Name of Patentee or Applicant of Cited Document
MT	AA	US - 5402415	03-28-1995	Jonathan S. Turner
	AB	US - 5229991	07-20-1993	Jonathan S. Turner
	AC	US - 5260935	11-09-1993	Jonathan S. Turner
	AD	US - 5339311	08-16-1994	Jonathan S. Turner
	AE	US - 5179556	01-12-1993	Jonathan S. Turner
	AF	US - 5179551	01-12-1993	Jonathan S. Turner
	AG	US - 4901309	2-13-1990	Jonathan S. Turner
	AH	US - 4849968	07-18-1989	Jonathan S. Turner
	AI	US - 4829227	05-09-1989	Jonathan S. Turner
	AJ	US - 4734907	03-29-1988	Jonathan S. Turner
	AK	US - 4494230	01-15-1985	Jonathan S. Turner
	AL	US - 4491945	01-01-1985	Jonathan S. Turner
	AM	US - 4630260	12-16-1986	Toy et al.
	AN	US - 4893304	01-09-1990	Giacopelli et al.
	AM	US - 5127000	06-30-1992	Michel A. R. Henrion
	AN	US - 5173897	12-22-1992	Schrodi et al.
	AO	US - 5253251	10-12-1993	Toshiya Aramaki
	AP	US - 5842040	11-24-1998	Hughes et al.

EXAMINER'S INITIALS	Cite No.	OTHER DOCUMENTS
PT	AQ	ZUBIN DITTIA, "Integrated Hardware/Software Design of a High Performance Network Interface," March 2000, Doctor of Science Thesis, Sever Institute of Technology, Washington University, St. Louis, Missouri, 139 pages.
	AR	JONATHAN S. TURNER, "An Optimal Nonblocking Multicast Virtual Circuit Switch," June 1994, Proceedings of Infocom, 8 pages.
	AS	CHANEY ET AL., "Design of a Gigabit ATM Switch," Feb. 5, 1996, WUCS-96-07, Washington University, St. Louis, MO, 20 pages.
	AT	TURNER ET AL., "System Architecture Document for Gigabit Switching Technology," Aug. 27, 1998, Ver. 3.5, ARL-94-11, Washington University, St. Louis, MO, 110 pages.

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	BA	GEORGE VARGHESE and ANTHONY LAUCK, "Hashed and Hierarchical Timing Wheels: Efficient Data Structures for Implementing a Timer Facility," IEEE/ACM Transactions on Networking, Vol. 5, No. 6, December 1997, pp. 824-834.			